

Receiver-Exciter Controller Design

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A description of the general design of both the Block III and Block IV Receiver-Exciter Controllers for the Deep Space Network (DSN) Mark IV-A System is presented along with the design approach.

I. Introduction

Two Receiver-Exciter Controllers (RECs) are being developed as part of the DSN Mark IV-A System implementation for the Receiver-Exciter Subsystem (RCV). One controller is designed to control DSS Block III RCV hardware and is known as the Block III REC. The other controller is designed to control DSS Block IV RCV hardware and is known as the Block IV REC. The Block III REC is designed for use at the following three types of antenna sites:

- | | |
|----------------------------------|----------------|
| (1) 9-meter track and telemetry | (S-band) |
| (2) 34-meter track and telemetry | (S- or X-band) |
| (3) 34-meter listen-only | (S- or X-band) |

The Block IV REC is designed for use at the 64-meter track and telemetry antenna sites. Associated with each Block III REC and Block IV REC is an instrumentation controller and various supporting hardware assemblies.

In accordance with established general DSN requirements, these controllers are designed to enable the Receiver-Exciter Subsystem (RCV) to be configured, calibrated, initialized and operated from a central location via high-level instructions. This is being accomplished by designing the RECs to be operated under the control of the DMC subsystem. The high-level instructions are in the form of standard subsystem

blocks (SSBs) received via the local area network (LAN). The centralized control provided by these RECs and other DSCC controllers in Mark IV-A is intended to reduce DSN operations costs from the Mark III era.

II. Design Approach and Guidelines for Implementation

The design approach being used on the RECs as regards to commonality, interfaces and standards is discussed below.

The RECs are designed so as to provide maximum commonality in both hardware and software. Both RECs use a similar chassis, boards, peripherals and instrumentation controller. Both RECs share the majority of software modules. Industry standard interfaces are used except where existing hardware design prevents it and commercially available products are used extensively.

All software is designed to comply with standards established for (a) general data flow, (b) data interchange, and (c) man-machine interface. The software functional capabilities are based on the Consolidated Requirements for DSCC Subsystems Interfacing with DMC in addition to the RCV functional requirements document and general DSN requirements. The software is being developed using strict software engineering practices and a top-down approach.

III. Design

The design of both the Block III REC and the Block IV REC incorporates the following functional capabilities:

- (1) RCV and REC initialization.
- (2) Interfaces to the following subsystems via the LAN:
 - (a) DSCC Monitor and Control Subsystem (DMC).
 - (b) Antenna Pointing Subsystem (APS).
 - (c) Precision Power Monitor (PPM).
 - (d) Tracking Subsystem (TRK).
- (3) Automated control of RCV configuration.
- (4) Automated control of acquisition and tracking of downlink signal based on predicts.
- (5) Automated control of frequency generation of uplink signal.
- (6) Automated control of pretrack and posttrack calibration.
- (7) Status monitoring of all controlled functions resulting in spontaneous generation of messages indicating alarm conditions and periodic monitor data blocks to DMC.
- (8) Diagnostic procedures.
- (9) Controller self-testing and monitoring.
- (10) An interface to the Maintenance Support Assembly (MSA).

Details of the exact implementation of these functions will be left to future progress reports. This report will discuss only the implementation of configuration in any detail.

A. Hardware Design

1. **Block IV REC.** In addition to the REC itself, other special-purpose hardware is required to fully automate the Block IV RCV. Fortunately, in the Block IV RCV much of this hardware already exists. A block diagram of the Block IV REC and its peripherals is shown in Fig. 1. A brief description of each item in the block diagram follows.

The Block IV REC hardware design is based on the Computational and Control Modules (CCM) standard chassis designed by R. Reynolds. This chassis features a 12-slot multi-bus card cage and a power supply. The front panel contains only an ON/OFF switch, a RESET button and an RS-232C port for the MSA. The port is used only for testing and diagnostic purposes. The back panel contains ports for the follow-

ing four types of interfaces: RS-232C, IEEE-488, SIA and, TTL.

A partial list of boards used within the Block IV REC includes the following:

- (1) Two 8086-based CPU boards.
- (2) A serial communications board.
- (3) A programmable I/O board.
- (4) An IEEE-488 interface board.
- (5) An SIA interface board.
- (6) A core memory board (nonvolatile).
- (7) An expansion PROM board.

Current plans provide for 96K bytes of PROM, 32K bytes of core memory and 64K bytes of on-board RAM.

The decision to use two CPU boards within the RECs was based on several factors. First, the Exciter Synthesizer Controller (DCO) transmits data whenever it wants and it must have an "immediate listening ear" to prevent loss of data. Second, communication with the DMC subsystem and other DSCC subsystems via the LAN requires considerable processor time and high responsiveness. Lastly, too much processor loading can cause timing problems, inability to respond in a timely manner, and degradation of RCV performance. The two CPU boards have been designated as the Control Processor (CP) and the I/O Processor (IOP), respectively. The IOP serves as a "slave" to the "master" CP. The two boards communicate with each other using their respective parallel ports (8255 chips).

The Instrumentation Controller (IC) is based upon the use of commercial equipment. It uses IEEE-488 interfaces throughout. A detailed block diagram of the IC and its peripherals is shown in Fig. 2. There are three digital voltmeters (DVM's), two of which are dedicated to measuring automatic gain control (AGC) from Receiver A and Receiver B respectively. The third DVM is used together with a multiplexer to measure 60 parameters in the Block III RCV such as static phase error (SPE), dynamic phase error (DPE), dynamic AGC, power monitor signals, etc. Nine different voltages are measured for the Block IV REC and are shown in the diagram. In addition, there is one frequency counter in the IC which is used to measure receiver VCO, doppler and synthesizer frequencies, etc.

The simulation (doppler) synthesizer is a programmable synthesizer which provides reference frequency for the extraction of doppler.

The Exciter Synthesizer Controller is known as the Digitally Controlled Oscillator (DCO). The DCO is an existing piece of hardware which was designed to monitor and control a Dana Frequency Synthesizer. The DCO accepts ASCII commands across an RS-232C data link and transmits parallel BCD frequency settings to the synthesizer. The DCO is capable of performing a variety of functions such as loading a series of up to 100 frequency rate and time pairs, generating status reports, and performing diagnostic tests.

The Exciter Configuration Control and Status Assembly (CCSA) is an existing piece of hardware which monitors and controls the Block IV exciter configuration. The Exciter CCSA communicates with the REC using an SIA interface and receives commands to establish various switch settings such as exciter drive, ranging and command modulation, doppler bias, etc.

The Receiver CCSA is also an existing piece of hardware and is used to monitor and control the configuration and status of both Receiver A and Receiver B in the Block IV RCV. The Receiver CCSA also communicates with the REC using an SIA interface. The Receiver CCSA receives commands to establish various switch settings such as receiver band, loop bandwidth, AGC bandwidth, telemetry bandwidth etc. It also provides receiver lock status to the REC.

The Receiver Programmed Oscillator Control Assemblies (POCAs) are identical, existing pieces of hardware which are designed to monitor and control a Dana Frequency Synthesizer in Receiver A and Receiver B respectively. The POCAs communicate with the REC using an SIA interface and transmit parallel BCD frequency settings to the synthesizers. Each POCA is capable of storing up to four frequency rate and time pairs. It can also perform triangular sweeps when given a center frequency and corresponding upper and lower limits.

The time code translator provides a 27-bit binary data stream containing date and time from the Frequency and Timing Subsystem (FTS).

The Maintenance Support Assembly (MSA) is connected to the REC using an RS-232C interface and is used for maintenance and development purposes only. It has an ASCII keyboard and a CRT.

2. Block III REC. The Block III REC also requires additional special-purpose hardware to fully automate the Block III RCV. Some of this hardware is common to the Block IV REC. A block diagram of the Block III REC and its peripherals is shown in Fig. 3. A brief description of the hardware unique to the Block III REC follows.

The Block III REC also uses the CCM-standard chassis and has a front panel similar to the Block IV REC. The Block III REC back panel contains several more ports to accommodate the three types of configurations. There is extensive commonality in the use of boards within the controller with the following exceptions. The Block III REC does not require an SIA interface board but does require two additional programmable I/O boards and an optically isolated I/O board (for handling relay drivers).

The Exciter Configuration and Status Assembly (CSA) is a new piece of equipment designed to monitor and control the Block III exciter configuration. It has a special-purpose TTL interface with the REC. The exciter CSA is used to establish various switch settings such as exciter drive and ranging, test and command modulation.

Each receiver in the Block III RCV requires a receiver CSA to monitor and control its configuration. The receiver CSAs also have special-purpose TTL interfaces with the REC. The Receiver CSAs are used to establish various switch settings such as loop bandwidth, AGC bandwidth, telemetry bandwidth, etc. It also provides receiver lock status to the REC.

The S-X controller is an existing piece of hardware which is used to control various switches associated with S-band and X-band such as the S-X translator, receiver bandwidth (S or X), translator input, doppler bias, etc.

The phase shifters are unique to the 9-meter configuration of the Block III REC. They shift the phase of the reference to the angle channel phase detectors with respect to the reference (sum-channel) receiver. The REC sends an 8-bit value indicating how much shift is desired.

The output of the 10-MHz acquisition detector is a bit called acquisition trigger at zero crossing (ATZ). This bit indicates when the incoming 10-MHz IF signal is at zero-beat with the 10-MHz reference frequency. This bit is used in the REC to stop the receiver synthesizer sweep, unshort the receiver loop filter and allow the receiver to be phase-locked to the signal.

B. Software Design

The software design is based on the use of two 8086-based CPU boards and a Real-Time Multi-tasking Executive. Again, the two boards have been designated as the control processor and the I/O processor, respectively. The I/O processor serves as a "slave" to the "master" control processor.

Tasks have been formulated and assigned to one or both of the boards based on ports required as well as functional

grouping. A list of tasks assigned to the control processor and a brief description of each is given in Table 1 in order of highest to lowest priority. Similar information for the I/O processor is given in Table 2, again in order of highest to lowest priority. Some details of the implementation of the configuration task are discussed later in this section.

In addition to the tasks defined in Tables 1 and 2 there are several functions which must be interrupt-driven. Interrupt service routines for these types of functions are listed below for each processor board in order of highest to lowest priority.

Control processor

- Power-on, reset.

- Functionally Independent Data flow Module (FIDM).

- FTS date/time read.

- Executive time-out timer.

I/O processor

- Power-on, reset.

- DCO service request.

- MSA service request.

- I/O executive.

- Instrumentation controller communications.

The FIDM is used to implement Level 3 of the LAN protocol.

The configuration task is executed partly in the control processor and partly in the I/O processor. A functional flow for this task is given in Fig. 4. This task begins with the receipt

of a controller directive SSB from the DMC subsystem containing a configuration directive. At this point, the directive must have been correctly transmitted across the LAN and received in the REC, using FIDM. The checksum for the SSB is computed and verified in FIDM. Processing continues as the SSB is decoded and the directive is parsed and validated. If the directive is valid, the directive response SSB indicates that the directive was accepted. Otherwise, the directive response indicates that the directive was rejected. All of the processing up to this point is done in the control processor. Then the specified configuration parameters are passed to the I/O processor (IOP). The IOP then builds and sends commands to the indicated hardware assembly or assemblies. The IOP reads the status of the hardware assemblies and verifies that the specified configuration has been reached. Then the IOP notifies the control processor of the status of the directive — either normal completion or error condition. Finally, the control processor builds and sends an event notification SSB to the DMC subsystem to indicate the results of the directive execution. The SSB is sent across the LAN using FIDM again, of course.

IV. Future Plans

The requirements documents have been written and the general design phase of the Block III and Block IV Receiver-Exciter Controllers is nearing completion. The detailed design phase is about to begin and the writing of the SDDs is in progress. Coding and unit testing of all software modules is scheduled for completion in January 1983. A three-phased integration testing period is planned with final delivery of the controllers including firmware and associated documentation at the end of June 1983.

Acknowledgments

The design of the Receiver-Exciter Controllers is the result of the work of several key individuals. The Block III RCV CDE is R. Weller and the Block IV RCV CDE is E. Serhal. Members of the Receiver-Exciter Controller development team whose contributions are acknowledged are J. Child, J. Estrada, G. Klein, P. Knowlton, K. Krauter, J. Nelson, and S. Ritchie.

Table 1. Tasks assigned to the control processor

Task	Description
Decode SSBs	Validate: source process code, SSB type, directive code and format (if applicable); activate appropriate task
Initialize controller	Check ports, boards, memory, registers; activate real-time executive
Monitor health	Perform continuous checkout of controller
Real-time processes (displays, MDTL)	Provide continuously updated data to all active displays and monitor data transfer lists (MDTLs)
Configure	Send configure commands to I/O processor
Acquire	Generate command stream for uplink and downlink acquisition and send to I/O processor
Display graphics	Build display graphics SSBs, activate real-time processes
Monitor data request	Send requested monitor data segment to requestor
Update data base	Place latest data from hardware assemblies into MDTL
Diagnostics	Execute requested diagnostic routine(s)
Halt/Idle	Halt controller; forward command to I/O controller

Table 2. Tasks assigned to the I/O processor

Task	Description
Halt/idle	Halt designated process or assembly
Initialize controller	Check ports, boards, memory, registers; wait for control processor commands
Initialize hardware assemblies	Place designated assembly into INIT configuration
Calibrate	Coordinate test signal and instrumentation controller to perform calibration
Monitor health	Perform periodic checks of processor and hardware assembly status
Real-time process (performance)	Check performance of subsystem (periodic)
Configure	Command and verify hardware assembly configuration
Acquire	Command and verify uplink and downlink acquisition
Diagnostics	Execute requested diagnostic routines

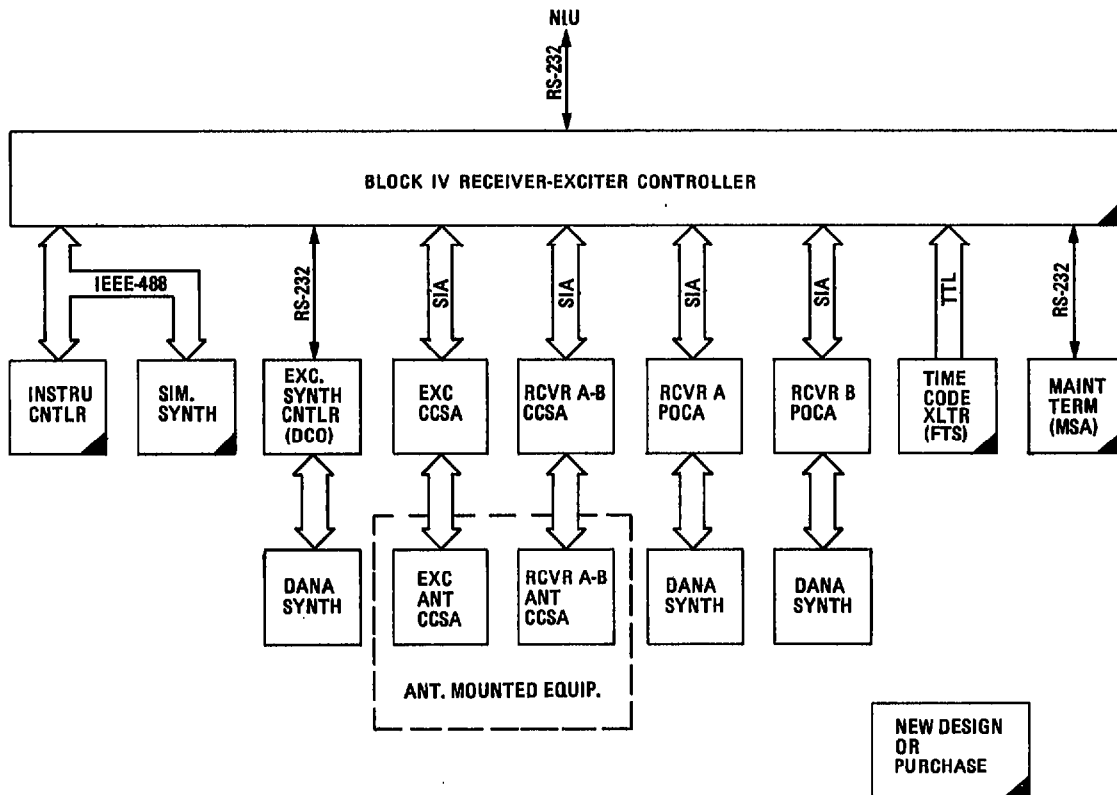


Fig. 1. Block IV Receiver-Exciter Controller block diagram

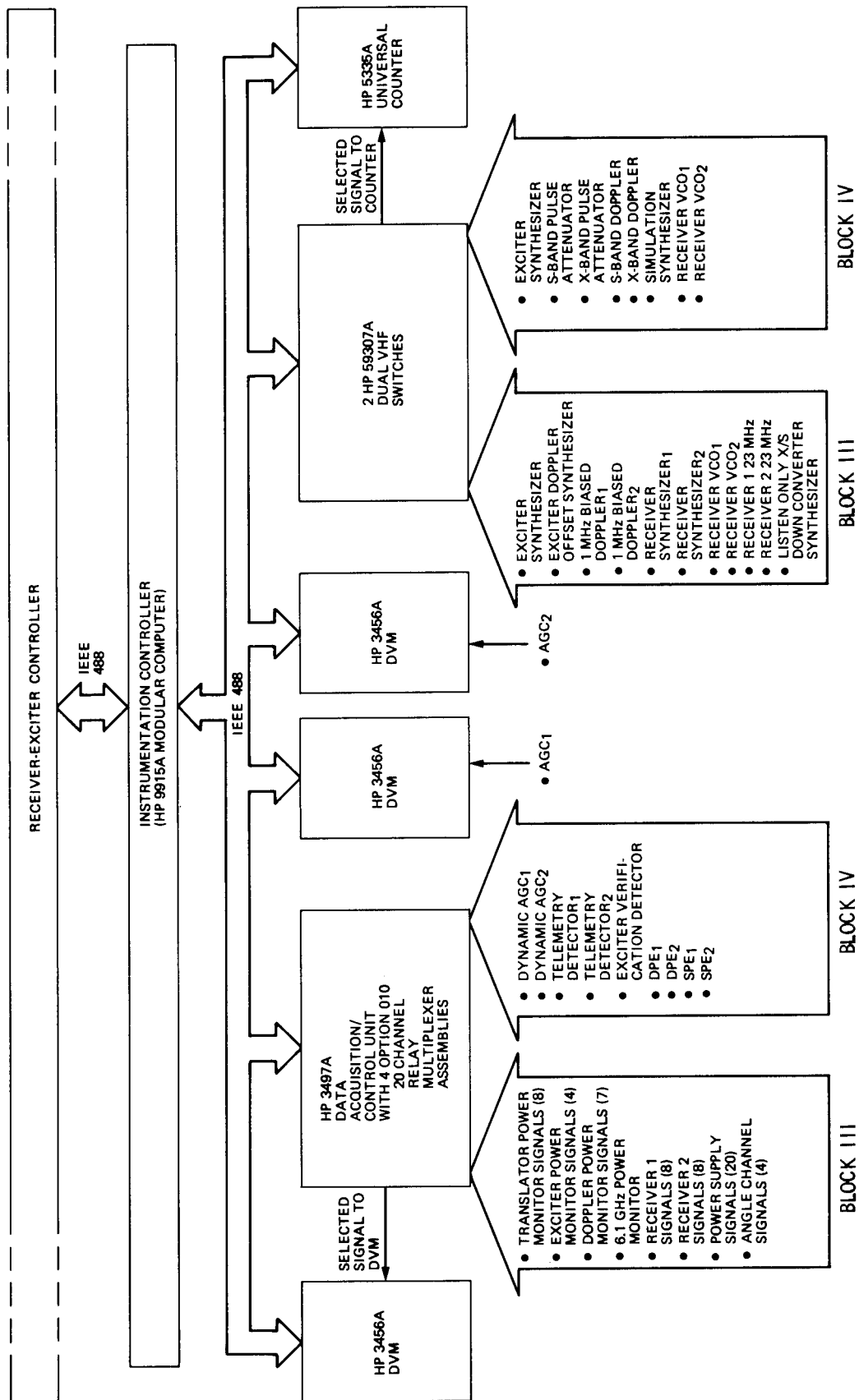


Fig. 2. Instrumentation Controller block diagram

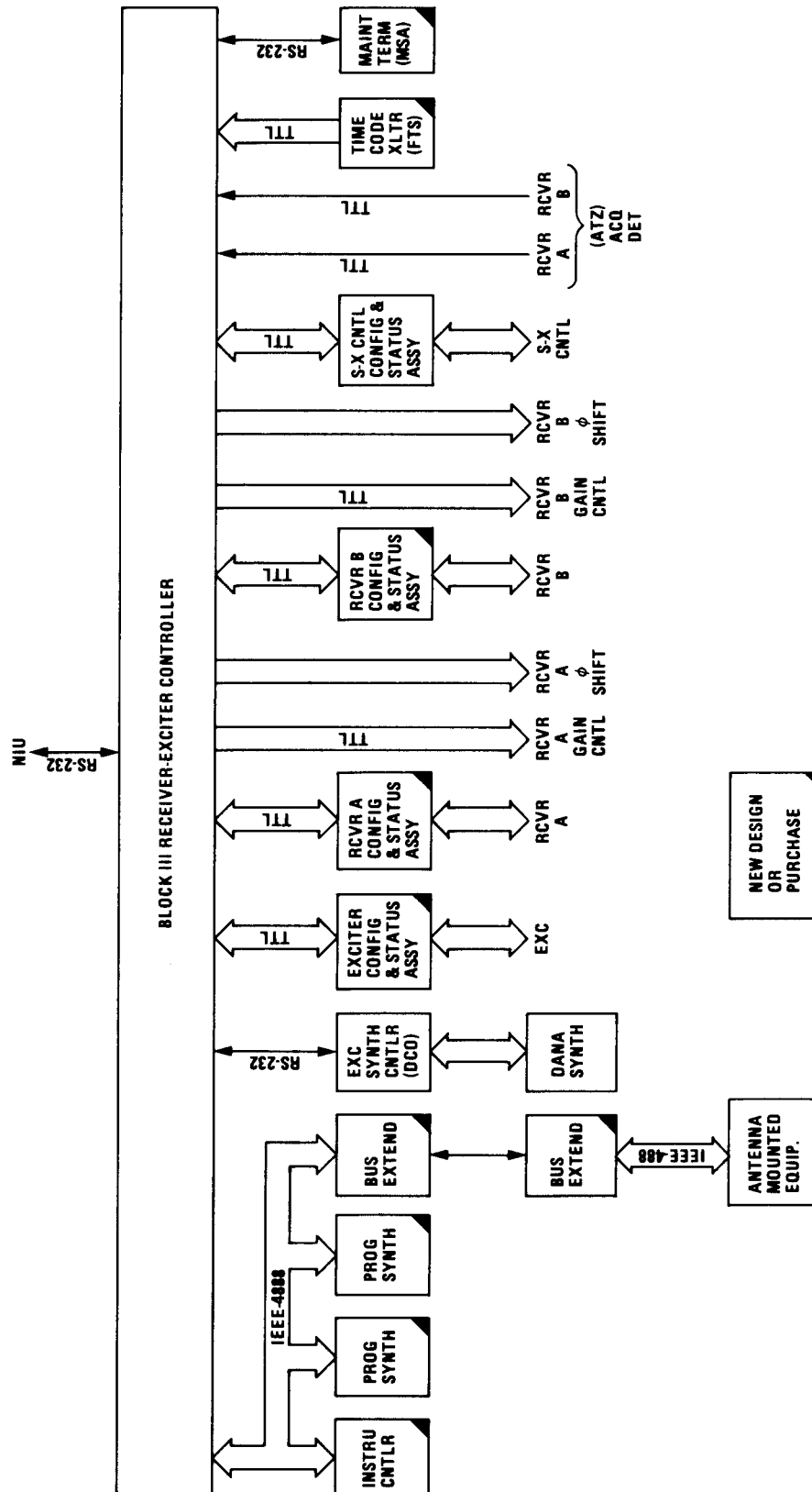


Fig. 3. Block III Receiver-Exciter Controller block diagram

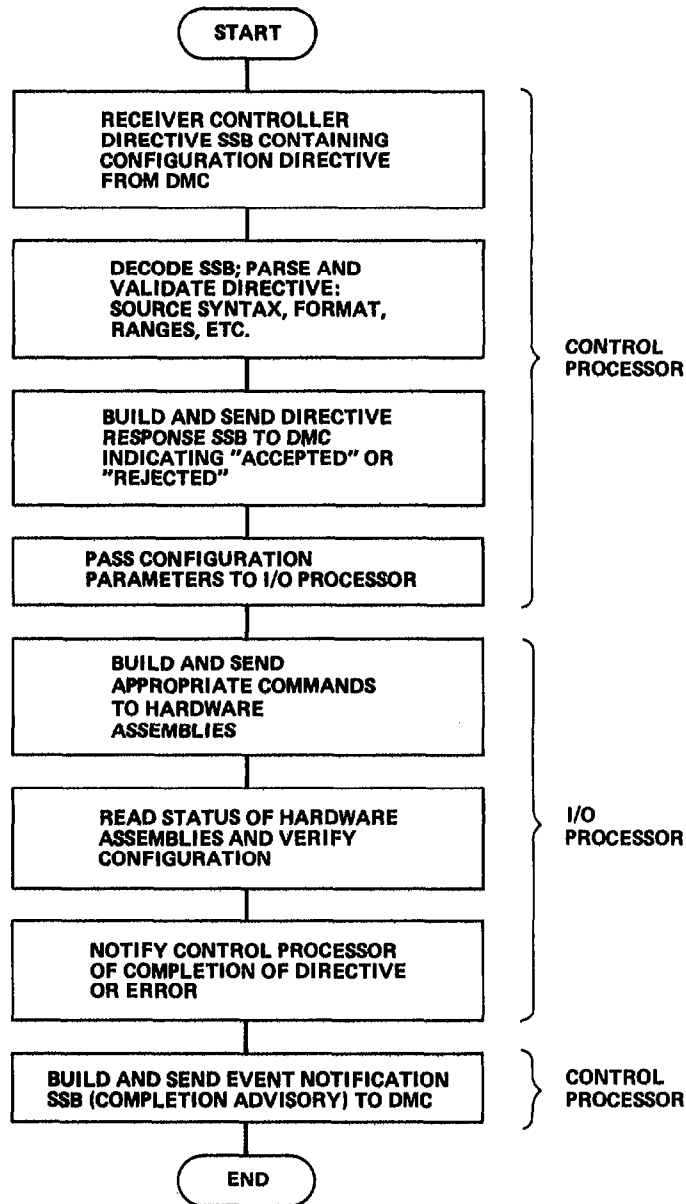


Fig. 4. Functional flow of configuration task